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Kyprianos Papadimitriou took his PhD, MSc, and Diploma from the Department of Electronic and Computer Engineering, Technical University of Crete, Greece. He is teaching Computer Architecture, and for several years he has been involved in the laboratory assignments of Logic Design, Digital Computers, Computer Architecture, and Design of VLSI/ASIC Systems. In the earliest years of his career he worked in the industry on the hardware design and implementation of the first version of Bluetooth technology (1.0). After his MSc, he started a spin-off company for commercializing a motion detection device for people with disabilities. He has worked as teaching staff at the School of Electrical and Computer Engineering of the Technical University of Crete, and as research associate at the Foundation of Research and Technology Heraklion and at the Technological Educational Institute of Crete. He has several scientific publications and 1 US patent, and he is reviewing for top scientific journals and conferences (ACM Transactions on Embedded Computing Systems, IEEE Transactions on VLSI Systems, IEEE Embedded Systems Letters, ELSEVIER Microelectronics Journal, IET Signal Processing, IEEE FPL, IEEE ReConFig, ARC, ReCoSoC).

RESEARCH INTERESTS

His research interests lie in the areas of Computer Hardware with a focus on Reconfigurable Computing (FPGAs), Embedded Systems, Application Acceleration, Reliability, and Networks-on-Chip. One of his PhD articles published in 2011 in the ACM Transactions on Reconfigurable Technology and Systems (ACM TRETS) is listed in the top-3 cited articles since this journal was launched (2008); ACM TRETS is the only scientific journal focusing on the field of reconfigurable computing.

PUBLICATIONS (2012-2018)

Journal Articles

1. G. Charitopoulos, I. Koidis, **K. Papadimitriou**, D. Pnevmatikatos, Run-Time Management of Systems with Partially Reconfigurable FPGAs, ELSEVIER, *Integration, the VLSI journal,* vol. 57, pp. 34-44, 2017.
2. D. Pnevmatikatos, **K. Papadimitriou**, T. Becker, P. Bohm, A. Brokalakis, K. Bruneel, C. Ciobanu, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M. D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste, FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration, *ELSEVIER Journal on Microprocessors and Microsystems (MICPRO)* - Embedded Hardware Design, 39(4-5), pp. 321-338, 2015.

3. M.D. Grammatikakis, **K. Papadimitriou,** P. Petrakis, A. Papagrigoriou, G. Kornaros, I. Christoforakis, O. Tomoutzoglou, G. Tsamis, M. Coppola, Security in MPSoCs: A NoC Firewall and an Evaluation Framework, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), special issue on Hardware Security and Trust,* 34(8), pp. 1344-1357, 2015.

4. **K. Papadimitriou**, A. Dollas, S. Hauck, Performance of Partial Reconfiguration in FPGA Systems: A Survey and a Cost Model, *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 4, no. 4, pp. 36:1-36:24, December 2011 **[in the top-3 cited articles of all time list of ACM TRETS].**

Book Chapters

5. M. Grammatikakis, H. Ahmadian, M. Coppola, S. Kavvadias, A. Mouzakitis, **K. Papadimitriou**, A. Papagrigoriou, P. Petrakis, V. Piperaki, M. Soulié, G. Tsamis, Chip-Level Communication Services, *Book Chapter in Distributed Real-Time Architecture for Mixed-Criticality Systems*, Taylor & Francis, 2018.

6. **K. Papadimitriou**, S. Thomas, A. Dollas, An FPGA-based Real-time System for 3D Stereo Matching, Combining Absolute Differences and Census with Aggregation and Belief Propagation, *Springer Book, extended versions of selected papers (after peer-review) from the 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC),* pp. 168-187, 2013.

Peer-reviewed Conference Papers

7. S. Khan, **K. Papadimitriou**, G. Buttazzo, K. Kalaitzaikis, A Reconfigurable PID Controller, in the Proceedings of *International Symposium on Applied Reconfiguralbe Computing (ARC)*, Santorini, Greece, May 2018.

8. P. Petrakis, M. Abuteir, M. D. Grammatikakis, **K. Papadimitriou**, R. Obermaisser, Z. Owda, A. Papagrigoriou, M. Soulie, M. Coppola, On-Chip Networks for Mixed-Criticality Systems, in the Proceedings of *27th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, London, UK, July 2016.

9. M. D. Grammatikakis, **K. Papadimitriou**, P. Petrakis, M. Coppola, M. Soulie, Address Interleaving for Low-cost NoCs, in the Proceedings of *International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC),* Tallinn, Estonia, June 2016.

10. G. Tsamis, S. Kavvadias, A. Papagrigoriou, M. Grammatikakis, **K. Papadimitriou**, Efficient Bandwidth Regulation at Memory Controller for Mixed Criticality Applications, in the Proceedings of *International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC),* Tallinn, Estonia, June 2016.

11. **K. Papadimitriou**, P. Petrakis, M. D. Grammatikakis, M. Coppola, Security Enhancements for Building Saturation-free, Low-Power NoC-based MPSoCs, in the Proceedings of *IEEE Workshop on Security and Privacy in Cybermatics (SPiCy), in conjunction with the IEEE Conference on Communications and Network Security (CNS),* pp. 594-600, Florence, Italy, September 2015.

12. G. Charitopoulos, D. Pnevmatikatos, M.D. Santambrogio, **K. Papadimitriou,** D. Pau, A Run-Time System for Partially Reconfigurable FPGAs: The case of STMicroelectronics SPEAr board, in the Proceedings of *Symposium on Parallel Computing with FPGAs (ParaFPGA), in conjunction with the International Conference on Parallel Computing (ParCo)*, pp. 553-562, Edinburgh, UK, September 2015.

13. G. Charitopoulos, I. Koidis, **K. Papadimitriou**, D. Pnevmatikatos, Hardware Task Scheduling for Partially Reconfigurable FPGAs, *HiPEAC Workshop on Reconfigurable Computing (WRC)*, Amsterdam, Netherlands, January 2015.

14. M. D. Grammatikakis, **K. Papadimitriou**, P. Petrakis, A. Papagrigoriou, G. Kornaros, I. Christoforakis, M. Coppola, Security Effectiveness and a Hardware Firewall for MPSoCs, in the Proceedings of *6th*

IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms (M2A2), in conjunction with the 16th IEEE International Conference on High Performance Computing and Communications (HPCC), pp. 1032-1039, Paris, France, August 2014.

15. C. Vatsolakis, **K. Papadimitriou**, D. Pnevmatikatos, Enabling Dynamically Reconfigurable Technologies in Mid Range Computers Through PCI Express, *HiPEAC Workshop on Reconfigurable Computing (WRC)*, Vienna, Austria, January 2014.

16. G. Rematska**, K. Papadimitriou**, A. Dollas, A Low-Cost Embedded Real-Time 3D Stereo Matching System for Surveillance Applications, in the Proceedings of *IEEE International Symposium on Monitoring and Surveillance Research (ISMSR), in conjunction with the IEEE International Conference on Bioinformatics and Bioengineering (BIBE),* Chania, Greece, November 2013.

17. S. Thomas, **K. Papadimitriou**, A. Dollas, Architecture and Implementation of Real-Time 3D Stereo Vision on a Xilinx FPGA, in the Proceedings of *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 186-191, Istanbul, Turkey, October 2013 [**nominated for best paper award; selected amongst 6 papers out of 249 submissions**].

18. C. B. Ciobanu, **K. D. Papadimitriou**, D. N. Pnevmatikatos, G. N. Gaydadjiev, FASTER Run-Time Reconfiguration Management, in the Proceedings of *ACM 27th International Conference on Supercomputing (ICS) Oregon,* pp. 463-464, US, June 2013.

19. **K. Papadimitriou**, D. Pnevmatikatos, A. Dollas, C. Koulamas, S. Aggelidakis, P. Chatzidakis, L. Vasilikiotis, M. Emmanouilidou, Developing RFID-based Systems for Security in Marine Transportations, in the Proceedings of *Panhellenic Conference on Informatics (PCI),* pp. 50-55, Athens, GR, October 2012.

20. D. Pnevmatikatos, T. Becker, A. Brokalakis, K. Bruneel, G. Gaydadjiev, W. Luk, **K. Papadimitriou**, I. Papaefstathiou, O. Pell, C. Pilato, M. Robart, M. D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration, in the Proceedings of *Euromicro Conference on Digital System Design (DSD)*, pp. 234-241, Cesme, Izmir, Turkey, September 2012.

Invited Conference Papers

21. G. Charitopoulos, I. Koidis, **K. Papadimitriou**, D. Pnevmatikatos, Hardware Task Scheduling for Partially Reconfigurable FPGAs (invited), in the Proceedings of *International Symposium on Applied Reconfigurable Computing (ARC),* pp. 487-498, Bochum, Germany, April 2015.

22. G. Charitopoulos, **K. Papadimitriou**, D. Pnevmatikatos, Run-Time Hardware Task Scheduling for Partially Reconfigurable FPGAs, in the poster session of *International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES)*, July 2014.

23. D. N. Pnevmatikatos, T. Becker, A. Brokalakis, G. N. Gaydadjiev, W. Luk, **K. Papadimitriou**, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M. D. Santambrogio, D. Sciuto, D. Stroobandt, Effective Reconfigurable Design: The FASTER Approach (invited, EU-funded projects session), in the Proceedings of *International Symposium on Applied Reconfigurable Computing (ARC),* pp. 318-323, Vilamoura, Portugal, April 2014.

24. M. D. Santambrogio, C. Pilato, D. Pnevmatikatos, **K. Papadimitriou**, D. Stroobandt, D. Sciuto, The FASTER Vision for Designing Dynamically Reconfigurable Systems (invited), in the Proceedings of *IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 5-8, Pavia, Italy, May 2013.

25. **K. Papadimitriou,** C. Pilato, D. Pnevmatikatos, M. D. Santambrogio, C. Ciobanu, T. Todman, T. Becker, X. Niu, T. Davidson, G. Gaydadjiev, W. Luk, D. Stroobandt, Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration (invited), in the Proceedings of *IEEE/IFIP International*

Conference on Embedded and Ubiquitous Computing (EUC), pp. 391-398, Paphos, CY, December 2012.

26. M. D. Santambrogio, D. Pnevmatikatos, **K. Papadimitriou**, C. Pilato, G. Gaydadjiev, D. Stroobandt, T. Davidson, T. Becker, W. Luk, D. Sciuto, Smart Technologies for Effective Reconfiguration: The FASTER Approach, in the Proceedings of *IEEE International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC),* York, UK, July 2012.

27. **K. Papadimitriou**, C. Vatsolakis, D. Pnevmatikatos, Acceleration of Computationally-Intensive Kernels in the Reconfigurable Era (invited), in the Proceedings of *IEEE International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*, York, UK, July 2012.